**Integration Manual**

**For**

**CF14 PSA Torque Arbitrator**

**VERSION: 5.0**

**DATE: 13-Feb-2018.**

**Prepared By:**

**Krzysztof Byrski,**

**Nexteer Automotive,**

**Saginaw, MI, USA**

**Revision History**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sl. No.** | **Description** | **Author** | **Version** | **Date** |
| 1 | Initial version | Sankardu Varadapureddi | 1.0 | 10-Mar-2015 |
| 2 | Updated for FDD v2.1.0 | Nick Saxton | 2.0 | 31-May-2016 |
| 3 | Updated for FDD v3.0.0 | Krishna Anne | 3.0 | 23-Feb-2017 |
| 4 | Updated for FDD v4.1.0 | Mateusz Bartocha | 4.0 | 20-Sep-17 |
| 5 | Added PSATA\_Per1 Scheduling Requirements | Krzysztof Byrski | 5.0 | 13-Feb-2018 |

**Table of Contents**

[1 Abbrevations And Acronyms 4](#_Toc475717075)

[2 References 5](#_Toc475717076)

[3 Dependencies 6](#_Toc475717077)

[3.1 SWCs 6](#_Toc475717078)

[3.2 Global Functions(Non RTE) to be provided to Integration Project 6](#_Toc475717079)

[4 Configuration REQUIREMeNTS 7](#_Toc475717080)

[4.1 Build Time Config 7](#_Toc475717081)

[4.2 Configuration Files to be provided by Integration Project 7](#_Toc475717082)

[4.3 Da Vinci Parameter Configuration Changes 7](#_Toc475717083)

[4.4 DaVinci Interrupt Configuration Changes 7](#_Toc475717084)

[4.5 Manual Configuration Changes 7](#_Toc475717085)

[5 Integration DATAFLOW REQUIREMENTS 8](#_Toc475717086)

[5.1 Required Global Data Inputs 8](#_Toc475717087)

[5.2 Required Global Data Outputs 8](#_Toc475717088)

[5.3 Specific Include Path present 8](#_Toc475717089)

[6 Runnable Scheduling 9](#_Toc475717090)

[7 Memory Map REQUIREMENTS 10](#_Toc475717091)

[7.1 Mapping 10](#_Toc475717092)

[7.2 Usage 10](#_Toc475717093)

[7.3 Non RTE NvM Blocks 10](#_Toc475717094)

[7.4 RTE NvM Blocks 10](#_Toc475717095)

[8 Compiler Settings 11](#_Toc475717096)

[8.1 Preprocessor MACRO 11](#_Toc475717097)

[8.2 Optimization Settings 11](#_Toc475717098)

[9 Appendix 12](#_Toc475717099)

# Abbrevations And Acronyms

|  |  |
| --- | --- |
| **Abbreviation** | **Description** |
| DFD | Design functional diagram |
| MDD | Module design Document |
|  |  |
|  |  |

# References

This section lists the title & version of all the documents that are referred for development of this document

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Title** | **Version** |
| 1 | MDD Guidelines | 1.3 |
| 2 | Software Naming Conventions | 1.2 |
| 3 | Software Design and Coding Standards | 2.1 |
| 4 | FDD - CF14 PSA Torque Arbitrator | 5.0.0 |
| 5 | Integration Manual Template.doc | 1.2 |

# Dependencies

## SWCs

|  |  |
| --- | --- |
| **Module** | **Required Feature** |
| **None** |  |

## Global Functions(Non RTE) to be provided to Integration Project

None

# Configuration REQUIREMeNTS

## Build Time Config

|  |  |  |
| --- | --- | --- |
| **Modules** | **Notes** |  |
| **None** |  |  |

## Configuration Files to be provided by Integration Project

None

## Da Vinci Parameter Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Notes** | **SWC** |
| **None** |  |  |

## DaVinci Interrupt Configuration Changes

|  |  |  |  |
| --- | --- | --- | --- |
| **ISR Name** | **VIM #** | **Priority Dependency** | **Notes** |
| **None** |  |  |  |

## Manual Configuration Changes

|  |  |  |
| --- | --- | --- |
| **Constant** | **Notes** | **SWC** |
| **None** |  |  |

# Integration DATAFLOW REQUIREMENTS

## Required Global Data Inputs

Refer FDD

## Required Global Data Outputs

Refer FDD

## Specific Include Path present

No

# Runnable Scheduling

This section specifies the required runnable scheduling.

|  |  |  |
| --- | --- | --- |
| **Init** | **Scheduling Requirements** | **Trigger** |
| **PSATA\_Init1** | None | RTE( Init) |

|  |  |  |
| --- | --- | --- |
| **Runnable** | **Scheduling Requirements** | **Trigger** |
| **PSATA\_Per1** | Shouble be executed after SF020A PosnTrakgServo and before SF004B Assist Summation and Limiting | RTE (2ms) |

# Memory Map REQUIREMENTS

## Mapping

|  |  |  |
| --- | --- | --- |
| **Memory Section** | **Contents** | **Notes** |
| **PSATA\_START\_SEC\_VAR\_CLEARED\_BOOLEAN**  **PSATA \_START\_SEC\_VAR\_CLEARED\_16**  **PSATA \_START\_SEC\_VAR\_CLEARED\_32**  **PSATA\_START\_SEC\_VAR\_CLEARED\_UNSPECIFIED** |  |  |
|  |  |  |

\* Each …START\_SEC… constant is terminated by a …STOP\_SEC… constant as specified in the AUTOSAR Memory Mapping requirements.

## Usage

|  |  |  |
| --- | --- | --- |
| **Feature** | **RAM** | **ROM** |
| **<Memmap usuage info>** |  |  |

Table 1: ARM Cortex R4 Memory Usage

## Non RTE NvM Blocks

|  |
| --- |
| **Block Name** |
| **None** |

## RTE NvM Blocks

|  |
| --- |
| **Block Name** |
| **None** |

# Compiler Settings

## Preprocessor MACRO

None.

## Optimization Settings

None

# Appendix